# Bias-Stress Effect in 1,2-Ethanedithiol-Treated PbS Quantum Dot Field-Effect Transistors

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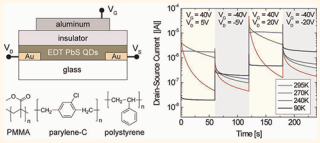
**ABSTRACT** We investigate the bias-stress effect in field-effect transistors (FETs) consisting of 1,2-ethanedithiol-treated PbS quantum dot (QD) films as charge transport layers in a top-gated configuration. The FETs exhibit ambipolar operation with typical mobilities on the order of $\mu_e = 8 \times 10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$ in n-channel operation and $\mu_h = 1 \times 10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$ in p-channel operation. When the FET is turned on in n-channel or p-channel mode, the established drain–source current rapidly decreases from its initial magnitude in a stretched exponential decay, manifesting the bias-stress effect. The choice of dielectric is found to have little effect on the characteristics of this bias-stress effect, leading us to conclude that the associated charge-trapping process originates within the QD film itself. Measurements of bias-stress-induced time-dependent decays in the drain–source current ($I_{DS}$) are well fit to stretched exponential functions, and the time constants of these decays in n-channel and p-channel operation are found to follow thermally activated (Arrhenius) behavior. Measurements as a function of QD size reveal that the stressing process in n-channel operation is faster for QDs of a smaller diameter while stress in p-channel operation is found to be relatively invariant to QD size. Our results are consistent with a mechanism in which field-induced nanoscale morphological changes within the QD film result in screening of the applied gate field. This phenomenon is entirely recoverable, which allows us to repeatedly observe bias stress and recovery characteristics on the same device. This work elucidates aspects of charge transport in chemically treated lead chalcogenide QD films and is of relevance to ongoing investigations toward employing these films in optoelectronic devices.




**KEYWORDS:** lead sulfide · quantum dot · ligand exchange · field-effect transistor · bias-stress effect

Although much progress has been made in advancing the performance of optoelectronic devices that incorporate colloidal quantum dot (QD) thin films, aspects of charge transport in these devices remain poorly understood. In several recent studies of lead chalcogenide QDs in field-effect transistor (FET) structures, a rapid bias-stress effect, or shift in threshold voltage ($\Delta V_T$) with the application of a gate bias, was observed.[1−6] This effect manifests as a stretched exponential decay in the drain–source current ($I_{DS}$) after a bias is applied to the gate electrode. The instability associated with bias stress precludes practical applications of QD FETs and complicates the interpretation of their performance characteristics. For example, in the case of alkanedithiol-treated PbSe QD FETs, the speed and extent of this decay necessitated Liu and co-workers to perform FET measurements as rapidly as possible (<500 ms) in order to minimize the distortion of transfer and output characteristics.[3]

The origins of the bias-stress effect have been extensively studied in the past two decades for FETs containing organic small-molecule,[7,8] conjugated polymer,[9−15] metal oxide,[16] and amorphous silicon (a-Si:H)[17,18] charge transport layers. In contrast, only a few reports directly address this phenomenon in QD FETs. In the case of PbSe QD FETs in which the QDs were passivated by either oleic acid,[1] alkanedithiols,[2,3,5,6] or amine ligands,[4] screening of the gate field by charge trapping at or near the semiconductor/dielectric interface was identified as the most likely mechanism for the bias-stress effect. In these studies, however, the dynamics of the stressing process were not quantitatively characterized and uncertainty remains regarding the nature of the trapped charge. In particular, it remains unclear whether the charge that screens the gate field accumulates in surface states at the QD/dielectric interface or within the QD film itself. In organic FETs, hydroxyl groups at the surface of $SiO_2$ have been implicated as electron-trapping sites[19] and surface-bound water molecules have been identified to act as hole traps.[15,20] On the other hand, the presence of QD surface defects[21−25] or the

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organic ligands intended to passivate QD surfaces[26−28] may also act as trapping sites.

In the present work, we investigate the origin of the bias-stress effect in 1,2 Ethanedithiol (EDT)-treated PbS QD FETs by studying the dynamics of the stressing process as a function of drain bias, gate bias, temperature, and QD size. In addition to a standard bottom-gate bottom-contact FET configuration, we utilize a top-gate bottom-contact configuration with a series of dielectric materials. Importantly, this approach provides a way to isolate the influence of the QD/dielectric interface on transistor performance and thereby enables the study of bulk properties of the QD film. We choose to study films of EDT-treated PbS QDs because they have been comparatively less well-studied in FET geometries than PbSe QDs yet have been central to several recent optoelectronic device demonstrations.[29−31] From the current−voltage response of the FETs, we find that top-gated structures exhibit ambipolar operation with typical mobilities on the order of $\mu_e = 8 \times 10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$ in n-channel operation and $\mu_h = 1 \times 10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$ in p-channel operation. The bias-stress characteristics are observed to be qualitatively similar to those reported in EDT-treated PbSe QD FETs.[3,5] A key observation is that the stress and recovery characteristics are similar in devices made with a series of different dielectrics, including parylene-C, poly(methyl methacrylate) (PMMA), and polystyrene, which suggests that charge trapping occurs within the QD film itself and is not due to interface states at particular QD/dielectric interface. The measurements of bias-stress-induced time-dependent decays in the drain−source current ($I_{DS}$) are fit well to stretched exponential functions, and the time constants of these decays in n-channel and p-channel operation are found to follow thermally activated Arrhenius behavior. Measurements as a function of QD size reveal that the stressing process in n-channel operation is faster for QDs of a smaller diameter while stress in p-channel operation is found to be relatively invariant to QD size. These results are consistent with a mechanism in which field-induced morphological changes within the QD film result in screening of the applied gate field.

## RESULTS AND DISCUSSION

For the fabrication of all FET structures described in this study, PbS QDs with a band-edge absorption peak at wavelength $\lambda$ = 1155 nm (corresponding to a QD energy gap of $E_g$ = 1.1 eV and a QD diameter of $d$ = 4.40 nm[32]) are used, unless otherwise specified. All fabrication and testing steps are carried out under rigorously air-free (nitrogen glovebox or vacuum chamber) conditions. We first consider FETs fabricated in a bottom-gate/bottom-contact configuration on Si/SiO$_2$ substrates. For these structures, QD films are cast onto substrates that are prepatterned with interdigitated source and drain electrodes, and a contact

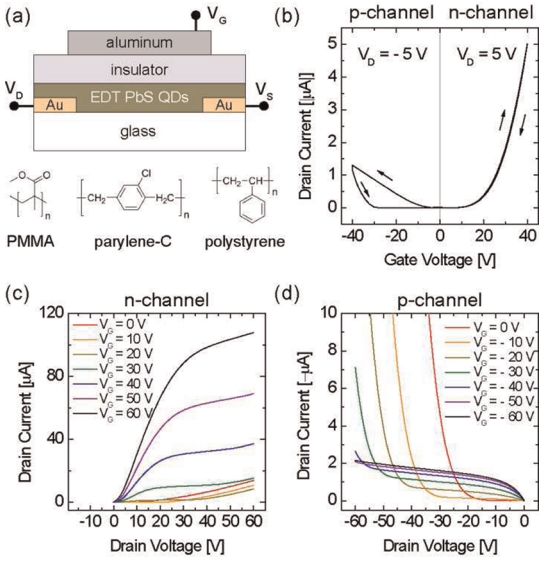


**Figure 1. (a) Schematic of device structure and molecular structures of parylene-C, PMMA, and polystyrene, which are used as gate dielectric materials. (b) Ambipolar transfer characteristics of a representative EDT PbS QD FET made with a PMMA dielectric. The p-channel and n-channel sweeps were measured separately and with a break of several minutes between in order to minimize distortion. (c,d) Output characteristics for positive and negative gate biases, respectively.**

to the underlying silicon gate is subsequently made (see Experimental Section for additional details). These devices exhibit ambipolar operation (see Figure S1 in the Supporting Information), consistent with recent reports on PbS[2] and PbSe QD-based FETs.[3] We note that, after the application of the gate bias, the $I_{DS}$ exhibits a stretched exponential decay on a time scale similar to that previously observed in PbSe QD FETs.[3,5]

To investigate whether the SiO$_2$ surface is responsible for the bias stress observed in these devices as well as to assess the role of the QD/dielectric interface in determining device performance, we next consider a series of top-gate/bottom-contact FETs with three different dielectrics: parylene-C,[7,33] PMMA,[34] and polystyrene.[35] Each of these dielectrics has been used in organic FET transistor studies specifically to avoid the formation of interface states associated with surfaces of SiO$_2$ dielectric layers. The device structure as well as the molecular structures for each of the dielectric materials used are shown in Figure 1a (see Experimental Section for details on device fabrication).

The output characteristics ($I_{DS}$ *versus* $V_D$) for a representative device that incorporates a PMMA dielectric layer are shown in Figure 1c,d for n-channel and p-channel operation, respectively. Saturation in the magnitude of drain−source current is observed for sufficiently high drain biases, corresponding to the pinch-off of the hole and electron channels. The transfer characteristics ($I_{DS}$ *versus* $V_G$) in the linear operating regime for the same device are shown in Figure 1b. To minimize the influence of bias stress on FET

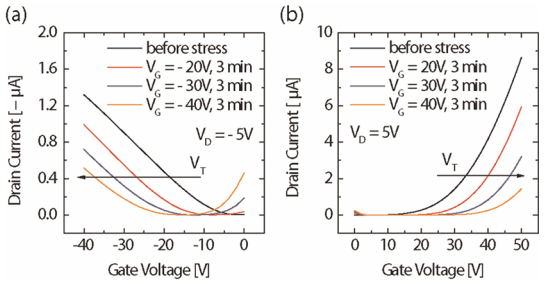


**Figure 2. (a,b) Transfer characteristics for a top-gated device that incorporates a PMMA dielectric in p-channel and n-channel operation, respectively, exhibiting a shift in threshold voltage, $\Delta V_T$, following sustained gate bias.**

characteristics, such as threshold voltage ($V_T$) and mobility ($\mu$), the single current–voltage sweeps are limited to <400 ms. Additionally, sweeps to positive and negative gate biases are conducted separately and with a break of several minutes between. To characterize threshold voltage and mobility, the initial sweep toward higher $|V_G|$ is used. We note that considerable hysteresis is observed in p-channel mode, while the forward and backward sweeps in n-channel mode are consistent. The value that we extract for the mobility in p-channel operation is thus likely to be an underestimation of the actual hole mobility in the device.

Threshold voltages for both n-channel and p-channel operation are extracted by extrapolating the $I_{DS}-V_G$ sweeps shown in Figure 1b to a current level of zero. Field-effect mobilities are then calculated assuming a linear drain–source current given by the following equation.[36]

$$I_{DS} = \left(\frac{W}{L}\right)\mu C_i(V_G - V_T)V_D \qquad (1)$$

The parameters $L$ and $W$ are the length and width of the FET channel, respectively, and $C_i$ is the dielectric capacitance (F cm$^{-2}$). We obtain mobilities of $\mu_e = 8 \times 10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$ in n-channel operation and $\mu_h = 1 \times 10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$ in p-channel operation (averaged over 8 devices). Similar ambipolar characteristics are observed in devices consisting of parylene-C and polystyrene dielectrics.

We next characterize the bias-stress effect in top-gated FET structures with different dielectric materials. We again first consider a representative FET with a PMMA dielectric. The threshold shift, $\Delta V_T$, is illustrated in Figure 2a,b for different stressing conditions. We note that for sufficiently high $|V_G|$ the slope of the transfer characteristic remains approximately unchanged with stress, indicating that carrier mobility remains largely unchanged by the stressing process. We also note that these shifts do not represent the ultimate $\Delta V_T$ reached during the stressing cycle due to a delay before acquiring the transfer curves, during which time the device is able to recover to an extent. To more accurately characterize the bias-stress effect,

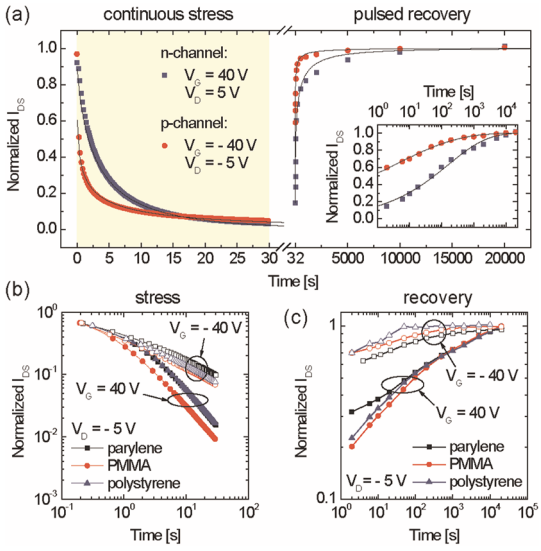


**Figure 3. (a) Normalized drain–source current under a continuous applied gate bias and recovery with time upon the release of that bias. Black lines are stretched exponential fits to the data. (Inset) Semilogarithmic plot of the recovery of normalized drain–source current following stress. (b,c) Normalized stress and recovery on log–log plots for devices made with different gate dielectrics at a drain bias of −5 V. Lines serve as a guide for the eye.**

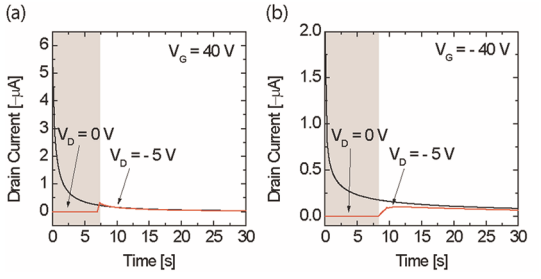


**Figure 4. Drain current of EDT-treated PbS QD FET with PMMA dielectric in n-channel (a) and p-channel (b) operation. The black curves represent measurements in which $V_G = \pm 40$ V and $V_D = -5$ V are applied simultaneously. The red curves represent measurements in which the application of $V_D$ is delayed by a mechanical switch. The delay is represented by the gray box.**

we measure the decay in $I_{DS}$ continuously under an applied gate bias. The decay in $I_{DS}$, normalized to its initial value, under an applied gate bias of $V_G = \pm 40$ V and drain bias of $V_{DS} = \pm 5$V, is shown in Figure 3a (see Experimental Section for additional details on this measurement). In <30 s, the currents in both n-channel and p-channel modes of operation decay by over an order of magnitude. We find that these decays occur regardless of whether or not a drain bias is applied to the device, as shown in Figure 4.

The decay in $I_{DS}$ is well fit by a stretched exponential function (fit to the data in Figure 3a is shown in black) of the form: $I_{stress}(t) = I_o \times \exp(-(t/\tau)^{\beta})$, where $I_o$ is the prestress drain–source current and $\tau$ and $\beta$ are the fitting parameters. Stretched exponential functions have been used extensively to characterize bias stress in various FET

systems,[7,15−18] in which $\tau$ is a characteristic time constant and $\beta$ is a dispersion parameter related to the distribution of time constants that characterize the trapping process. The decay in p-channel operation ($\tau$ = 0.7 s, $\beta$ = 0.38) is observed to occur faster than in n-channel operation ($\tau$ = 2.6 s, $\beta$ = 0.56). We note that, although the fitting parameter $\beta$ is similar to that observed in other systems, the time constant $\tau$ is faster by several orders of magnitude ($\tau \sim 10^3-10^8$ s for a variety of organic FETs).[15] For example, in pentacene-based FETs, the reported fitting values are $\beta \sim 0.4$ and $\tau \sim 10^4$ s.[7] One explanation for this difference is that trapping in the present QD system is relatively energetically favorable, whereas the long time constants for organic and a-Si:H FETs have been attributed to energy barriers that mediate the rate of trapping.[7,18]

The fast evolution of the bias-stress effect may suggest that there are a relatively large number of traps in the present system. To further assess this possibility, we estimate the amount of charge trapped during bias stress according to the equation $Q_{trapped} = C\Delta V_T$.[7,15] The value for $\Delta V_T$ is calculated from measurements of $I_{DS}$ under fixed bias conditions using the following equation:[10]

$$|\Delta V_T|(t) = \left(1 - \frac{I(t)}{I_o}\right)|V_G - V_{T0}| \qquad (2)$$

The parameter $I_o$ is the initial drain−source current, and $V_{T0}$ is the initial threshold voltage. $\Delta V_T$ is found to approach $V_G - V_{T0}$, which corresponds to a complete turn-off of the device. Our measurements suggest that there are at least 0.5 trapped charges per QD in both n-channel and p-channel operation (details of this calculation are available in the Supporting Information), which can reasonably be explained, for instance, by QD surface defects or excess ligands in the QD film.

The recovery of EDT-treated PbS QD FETs following the bias-stress condition is also shown in Figure 3a. These data are measured by periodically pulsing the gate bias from zero to $V_G$ and maintaining $V_G$ for only 10 ms to record $I_{DS}$. Recovery data are found to be well fit by a stretched exponential function of the form $I_{recovery}(t) = I_o \times (1 - \exp(-(t/\tau)^{\beta}))$. The recovery occurs faster after operation in p-channel mode ($\tau$ = 4 s, $\beta$ = 0.22) as compared to n-channel mode ($\tau$ = 163 s, $\beta$ = 0.36). At the first data point, collected at 2 s after the end of the stressing cycle, the hole current recovers to approximately 60% of its initial level. It subsequently approaches its initial value in a rapid, stretched exponential manner. Recovery from stress in n-channel operation, in contrast, is slower, taking several hours to fully return to its initial condition. This indicates that the detrapping of electrons in this system is slower than the detrapping of holes, suggesting the presence of deep electron traps and shallow hole traps. As shown in Figure 3b,c, stress and recovery characteristics are similar for devices made with all three dielectrics. We therefore conclude that the bias-stress effect in this system is a bulk phenomenon and not due to a particular QD/dielectric interface (*i.e.*, the charge accumulation that is responsible for the change in $I_{DS}$ occurs within the QD film itself).

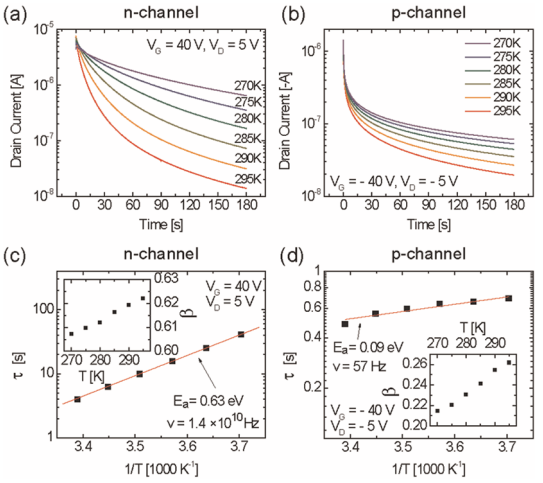


**Figure 5. (a,b) Drain current in n-channel and p-channel operation, respectively, as a function of time for different temperatures. (c,d) Stretched exponential fitting parameters as a function of inverse temperature. See text for definition of fitting parameters.**

To investigate the specific bulk mechanisms responsible for the bias-stress effect, transistor characteristics and measurements of the bias-stress effect were taken as a function of temperature ($T$ = 90−295 K). Samples were loaded into a Janis ST-100 optical cryostat and cooled with liquid helium. A cartridge heater controlled by a Lakeshore 330 temperature controller was used to maintain a desired temperature set point. Thirty minutes were allowed between stress measurements in order to allow the device to recover and for the temperature to stabilize at the next temperature point. The conductance in n-channel mode is found to be thermally activated, while meaningful characterization in p-channel mode is complicated by rapid hysteresis in the transfer characteristics, similar to a recent report by Kang and co-workers in PbSe QD FETs.[6] The transfer characteristics as a function of temperature are shown in Figure S5 of the Supporting Information.

The bias-stress effect is substantially diminished at reduced temperature, particularly in n-channel mode (see Figure 5a,b). We quantify these observations by extracting the stretched exponential fitting parameters from the normalized $I_{DS}$ decays at different temperatures, which are shown in Figure 5c,d. The time constant of the current decay, $\tau$, is found to follow thermally activated Arrhenius behavior of the form $\tau = \nu^{-1}\exp(E_a/k_BT)$, where $E_a$ and $\nu^{-1}$ are fitting parameters. Also, the dispersion parameter, $\beta$, is observed to slowly and linearly increase with temperature. Such temperature dependence has previously been noted in FETs based on several other material systems, including the polymer PTAA,[15] ZnO,[16] and amorphous

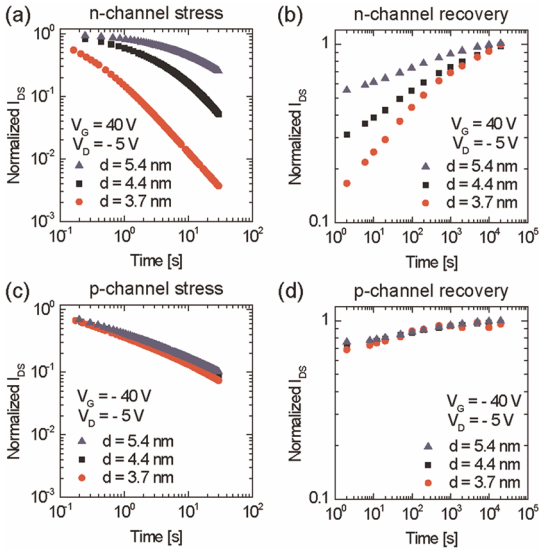


**Figure 6. Normalized drain–source current stress and recovery in n-channel (a,b) and p-channel (c,d) operation for devices made with PbS QDs of different core diameters.**

silicon (a-Si:H).[17,18] Bias stress in these systems was ascribed to defect creation within the semiconductor or dielectric layer; the activation energy can be interpreted as the energy required to create the trapping defects. In the present system, we determine the activation energy in n-channel mode to be 0.63 eV and the frequency prefactor, $\nu$, to be $1.4 \times 10^{10}$ Hz. These parameters are similar to those reported in organic and a-Si:H systems, where $E_a$ is typically ~0.6 eV and $\nu$ varies from $10^3$ to $10^9$ Hz.[15] In contrast, the relatively weak temperature sensitivity of the bias-stress effect in p-channel mode is described by the fitting parameters $E_a = 0.09$ eV and $\nu = 57$ Hz.

To further investigate the bulk mechanisms for bias stress, we study the effect of QD size on the bias-stress characteristics. The stress and recovery characteristics for devices made with QDs of 3.7, 4.4, and 5.4 nm diameters are shown in Figure 6. In n-channel operation, the time constant of $I_{DS}$ decay under bias stress is observed to decrease with QD size from 14.4 s for 5.4 nm QDs to 0.4 s for 3.7 nm QDs ($\beta \sim 0.5$). In p-channel operation, on the other hand, the speed of the decay is observed to be invariant to QD size. These observations may be understood in the context of the relative positions of the trap levels with respect to the conduction and valence bands. Several recent reports suggest that the HOMO level in PbS QDs is invariant with QD size relative to the LUMO level.[37,38] If the trap states present in the QD film are also isoenergetic with QD size, then the activation energy for hole trapping would be expected to remain constant. Conversely, since the electron trap depth will increase for smaller QDs, the activation energy may be expected to decrease, resulting in faster trapping and bias stress.

Regarding the physical origins for charge trapping within the QD film, it is known that QD surfaces harbor defects that may act as charge traps. Unpassivated cationic lead sites on the QD surfaces, for example, may be acting as electron traps while anionic sulfur sites may be acting as hole traps.[25,39] Our estimate of >0.5 trapped charges/QD, based on the magnitude of the threshold voltage shift during bias stress, can reasonably be explained by the presence of such defects. It is also possible that the electron traps in this system are related to oxide species ($PbSO_3$ and $PbSO_4$) that result from the oxidation of sulfur anions on the surfaces of the QDs.[40] We again note that rigorously air-free conditions were maintained throughout the synthesis of the QDs, as well as the fabrication and testing of the FETs, although we cannot rule out the presence of oxide compounds. We note, however, that the presence of any of these types of static defects alone would be insufficient to explain the dynamic and temperature-dependent nature of the observed bias-stress effect.

Analogous to trap creation mechanisms proposed to explain bias stress in other FET material systems including organic semiconductors,[15] ZnO,[16] and amorphous silicon (a-Si:H),[17,18] we propose that field-induced morphological changes within the QD film result in screening of the applied gate field, leading to the bias-stress effect. Such a mechanism would be consistent with the time-dependent and temperature-sensitive characteristics that we observe. As one possibility, bias stress may originate from the charge-induced ionization of EDT ligands when the gate bias is applied. In this case, injected charge carriers may induce the formation of ionic species within the QD film, such as thiolate molecules or protons, resulting in n-channel or p-channel bias stress, respectively. Here, the measured Arrhenius activation energies would correspond to the energies required to facilitate the creation of traps or, equivalently, the ionization of the ligands. A recent report on a bottom-gated organic FET consisting of the polymer, PTAA, describes an analogous mechanism wherein bias stress was attributed to the conversion of injected holes into protons in a reaction with water molecules at a $SiO_2$ surface.[20]

To explore the possible role that the ligands may be playing in bias stress, we characterized FETs consisting of QDs treated with a variety of different ligands. We observe qualitatively similar bias-stress characteristics for a set of four dithiols as well as mercaptoproprionic acid (MPA) (see Figure S7 in the Supporting Information). This indicates that the occurrence of bias stress is not highly sensitive to the particular surface treatment that is utilized, although we note that the functional group is similar among all of the ligands that we have explored. Finally, we note that the bias-stress effect in this system may also involve multiple different charge-trapping mechanisms occurring simultaneously within the QD film.

## SUMMARY

We characterized the performance of FETs consisting of 1,2-ethanedithiol (EDT)-treated PbS QD films and

studied the strong bias-stress effect observed in these devices. Top-gated devices exhibit ambipolar operation with typical mobilities on the order of $\mu_e = 8 \times 10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$ and $\mu_h = 1 \times 10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$. The particular choice of dielectric in the top-gate configuration was found to have little effect on the evolution of the bias-stress effect, leading us to conclude that the mechanism for bias stress originates in the bulk of the QD film and is not due to a particular semiconductor/dielectric interface. The extent of the bias-stress effect, as well as the very high speed of the stress and recovery processes that we observe, suggests that a large quantity of trapping states are available within EDT-treated PbS QD films. Measurements as a function of QD size reveal that the stressing process in n-channel operation is faster for QDs of a smaller diameter while stress in p-channel operation is found to be relatively invariant to QD size. Our results are consistent with a mechanism in which field-induced morphological changes within the QD film result in screening of the applied gate field. Possible specific physical mechanisms for bias stress were discussed. This work elucidates aspects of charge transport in chemically treated lead chalcogenide QD films and is of relevance to ongoing investigations toward employing these films in optoelectronic devices.

## EXPERIMENTAL SECTION

**Preparation of QD Films.** PbS QDs were synthesized according to a procedure described elsewhere.[41] The diameters of the QDs are estimated according to the position of their lowest energy absorption peaks ($\lambda$ = 939, 1155, and 1400 nm) to be 3.7, 4.4, and 5.4 nm, respectively.[32] The as-synthesized QDs were precipitated twice from solution with acetone and butanol and recast into hexane. Following a third crash-out, the QD precipitate was recast into octane at a concentration of 25 mg mL$^{-1}$. A single film was spun at 1500 rpm for 60 s to produce a ~15 nm thick film. The gold contacts at the edge of each sample were swabbed clear with octane to ensure good electrical access. The films were then treated in a solution of 0.1% EDT in acetonitrile (by volume) for 30 s followed by a short rinse in pure acetonitrile.

**Fabrication of FETs.** Gold interdigitated electrode arrays (with length and width of $L$ = 10 $\mu$m and $W$ = 12 mm, respectively) were fabricated on substrates of D263 borosilicate glass as well as on degenerately doped silicon with a 500 nm thermally grown $SiO_2$ layer. The electrode films were deposited by e-beam evaporation of 2.5 nm thick film of Ti followed by 45 nm thick film of Au and then patterned with liftoff. Following solvent cleaning, the substrates were subjected to oxygen plasma for 30 s. Glass substrates were submerged overnight in a 0.2 M solution of (3-mercaptopropyl)trimethoxysilane (MPTMS) in toluene to grow a self-assembled monolayer to promote adhesion of the QD films. After 1 min of sonication in isopropyl alcohol, the substrates were dried with nitrogen and transferred into a nitrogen environment for the deposition of the QD film. The gate dielectric was deposited as described below, and an aluminum gate was deposited by thermal evaporation through an aligned shadow mask. For the devices on $Si/SiO_2$ substrates, no surface treatment was employed prior to the deposition of the QD film. A contact to the underlying silicon was made by scoring through the top $SiO_2$ surface and applying a small amount of silver paste.

**Preparation of Dielectrics.** Films of parylene-C were formed using diX-C dimer from Daisan Kasei in a homemade CVD reactor. The deposition pressure of the vacuum system was approximately $10^{-3}$ Torr. Electronic grade polystyrene (Polymer Source Inc.) with $M_w$ = 221 500 and $M_w/M_n$ = 1.04 was dissolved in butyl acetate (50 mg/mL) and spin-cast at 2000 rpm. For poly(methyl methacrylate) dielectrics, 950 PMMA A4 resist, purchased from Microchem, was spin-cast at 1000 rpm. Following deposition of PMMA and polystyrene films, the samples were stored in an ultrahigh vacuum environment (~$10^{-8}$ Torr) overnight to remove solvent. Parylene-C, PMMA, and polystyrene film thicknesses were measured to be 478, 465, and 330 nm, respectively.

**Field-Effect Transistor Characterization.** To characterize the capacitance for each gate dielectric, test capacitors were made consisting of the identically prepared dielectric films sandwiched between an ITO bottom contact and an aluminum top contact. A Solartron 1260 impedance analyzer was then used to directly measure the gate capacitance at a frequency of $f$ = 37 Hz. The capacitances of the parylene-C, PMMA, and polystyrene films were measured to be 6.2, 5.7, and 5.9 nF cm$^{-2}$, respectively.

An Agilent 4156C semiconductor parameter analyzer was used to acquire transfer and output characteristics. For extraction of the field-effect mobility, the total stress time of transfer characteristic sweeps was limited to 400 ms.

For stress and recovery measurements, the Agilent 4156C was operated under computer control in order to ensure consistency of the measurement sequence. Several short (10 ms) pulsed measurements of drain−source current under the desired bias conditions were taken within a 2 h period before the application of the stress condition in order to ensure that the device was in an unstressed state and also to provide the initial drain−source current level for normalization. The current was measured continuously, while the gate bias was applied in order to capture the decay in current as the device became stressed. Immediately after, a series of pulsed measurements identical to the initial normalization current measurements tracked the recovery of the drain−source current level to its initial condition.

*Conflict of Interest:* The authors declare no competing financial interest.

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*Supporting Information Available:* Measurements on a bottom-gate/bottom-contact EDT-PbS QD FET, transfer characteristics on a semilog plot, stress measurements as a function of drain and gate bias, calculation of the density of trapped charge, charge transport measurements at low temperature, carrier mobility as a function of QD size, bias stress with other ligand treatments. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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